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(71) Applicant: ADVANCED MICRO DEVICES, INC. [US/US]; One AMD Place, Mail Stop 68, P.O. Box 3453, Sunnyvale, CA 94088-3453 (US).

(72) Inventors: MADRID, Philip, E.; 16642 Cordillera Drive, Round Rock, TX 78681 (US). MEYER, Derrick, R.; 2728 Creeks Edge Parkway, Austin, TX 78733 (US).

(74) Agent: DRAKE, Paul, S.; Advanced Micro Devices, Inc., 5204 East Ben White Boulevard, Mail Stop 562, Austin, TX 78741 (US).

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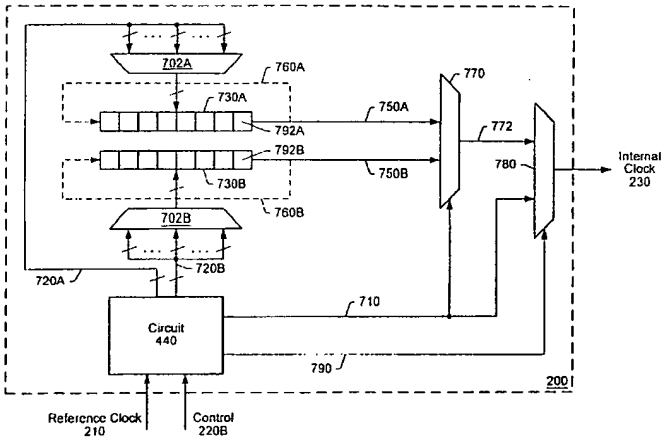

(57) Abstract: A method and mechanism for generating a clock signal with a relatively linear increase or decrease in clock frequency. A first clock signal is generated with a first frequency which is then used to generate a second clock signal with a second frequency. The second frequency is generated by dropping selected pulses of the first clock signal. Particular patterns of bits are stored in a storage element. Bits are then selected and conveyed from the storage element at a frequency determined by the first clock signal. The conveyed bits are used to construct the second clock signal. By selecting the particular pattern of bits selected and conveyed, the frequency of the second clock signal may be determined. Further, by changing the patterns of bits within the registers at selected times, the frequency of the second clock signal may be made to change in a relatively linear manner.

WO 2003/073244 A3

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